REMARKS

Favorable reconsideration of this application in view of the foregoing amendments and remarks to follow is respectfully requested.

Before addressing the specific grounds of rejection, Applicants have amended Claims 1, 10 and 17 by changing the term "a gate formed of a metal comprising Re" to "a Re-containing gate". This amendment, which is supported throughout the application, clearly defines the gate as containing Re and avoids unnecessary processing limitations within the claims.

Applicants have also amended Claims 1, 10 and 17 by changing the term "vertically abutting" to "located directly on a surface of". Thus, in the claimed structures, the Re-containing gate is in direct physical contact with the underlying gate dielectric. Support for this amendment to Claims 1, 10 and 17 is found throughout the originally filed application. See, for example, paragraph 0035 of the corresponding published application.

Applicants have further amended Claims 1, 10 and 17 to positively recite that that the *Re-containing gate has a work function ranging from about 4.6 eV to about 5.0 eV.* Support for this amendment to Claims 1, 10 and 17 is found in paragraph 0057 of the corresponding published application.

Since the above amendments to the claims are fully supported by the originally filed application, entry thereof is respectfully requested.

Claims 1, 2, 4, 7-11 and 14-16 stand rejected under 35 U.S.C. § 103 as allegedly unpatentable over U.S. Patent No. 6,476,545 to Suguro ("Suguro"), in view of U.S. Patent No. 6,300,208 to Talwar et al. ("Talwar et al.") and U.S. Patent No. 6,248,673 to Huang ("Huang"). Applicants respectfully disagree and submit the following.

Applicants submit that the applied prior art fails to render Applicants' invention unpatentable because the applied prior art fails to teach or suggest each and every limitation of Applicants' amended Claim 1. "To establish a prima facie case of obviousness of a claimed invention all the claimed limitations must be taught or suggested by the prior art". *In re Wilson,* 424 F.2d 1382, 1385, 165 USPQ 44, 496 (CCPA 1970). Amended Claim 1 recites:

> A metal oxide semiconductor (MOS) device comprising:
> a semi-conducting substrate having source and drain regions;
> a gate dielectric of less than 100 Å thickness on said semi-conducting substrate, said gate dielectric is selected from the group consisting of HfO_2, ZrO_3, Y_2O_3, silicates or nitrogen additions of HfO_2, ZrO_3, or Y_2O_3, and mixtures thereof; and
> a Re-containing gate located directly on a surface of said gate dielectric, said Re-containing gate has an interface trapped charge density of about 3E 10 cm^{-2} eV^{-1} to about 4E 10 cm^{-2} eV^{-1} and a work function that ranges from about 4.6 eV to about 5.0 EV, and wherein said Re-containing gate is derived from a $Re_2(CO)_{10}$ CVD precursor.

Applicants submit that the applied prior art fails to teach or suggest a structure that includes a Re-containing gate that is located directly on a surface of the gate dielectric and the Re-containing gate has a work function ranging from about 4.6 eV to about 5.0 eV, as recited in amended Claim 1. Applicants submit that the applied prior art also fails to teach or suggest Applicants' structures as recited in amended Claim 10 and 17, since the above-emphasized portion of Claim 1 is also present in Claims 10 and 17. Additionally, because the applied prior art fails to teach or suggest a gate structure including a Re-containing gate that is located directly on a surface of the gate dielectric, the applied prior art fails to teach or suggest a Re-containing gate having an interface trapped charge density of about 3E 10 cm^{-2} eV^{-1} to about 4E 10 cm^{-2} eV^{-1}, as recited in amended Claims 1, 10 and 17.

Referring to Page 2 of the present Office Action, the Examiner admits that Suguro fails to teach or suggest a gate conductor that is composed of Re. Applicants further note that the only

disclosure of a material selection to control the work function of the gate in the Suguro reference is found in Columns 11, 12 and Figures 7a and 7b, which disclose a metal nitride layer 61 being present between the gate electrode 62' and the gate dielectric layer 60. Therefore, because Suguro requires a metal nitride layer between the gate conductor and the gate dielectric in order to control the work function of the gate structure, in addition to failing to disclose Re as a material for the gate conductor, Suguro also fails to teach or suggest a structure in which the Re-containing gate is located directly on a surface of the gate dielectric and the gate has a work function ranging from about 4.6 eV to about 5.0 eV, as required by amended Claims 1, 10 and 17. Finally, because Suguro fails to teach or suggest that the Re metal gate is in direct physical contact with, i.e., located directly on a surface of, the gate dielectric, Suguro fails to teach or suggest a Re-containing gate having an interface trapped charge density of about 3E 10 cm^{-2} eV^{-1} to about 4E 10 cm^{-2} eV^{-1}, as recited in amended Claims 1, 10 and 17.

Therefore, because Suguro fails to teach or suggest at least three limitations of Applicants' claimed structure, as recited in amended Claims 1, 10 and 17, Suguro does not render Applicants' invention unpatentable.

Applicants respectfully submit that the combination of Talwar et al. and Huang does not obviate the above defects in Suguro, since none of the applied secondary references teaches or suggests Applicants' claimed structures. Referring to Pages 2 and 3 of the present Office Action, in order to meet the limitation of a Re metal gate, which the Examiner has admitted is not present in Suguro, the Examiner alleges that Talwar et al. discloses a Re metal gate that meets the limitations of Applicants' claims. Applicants submit that Talwar et al. is far removed from Applicants' claimed invention, since Talwar et al. discloses a method in which the source

and drain regions of a device are activated using a laser anneal that allegedly does not subject the gate region of the device to high temperature processing.

The portion of the Talwar et al. reference that the Examiner cites to meet the limitation of Applicants' claimed gate structure is merely a list of materials that may be used to provide a metal gate. Talwar et al. does not disclose a Re-containing gate *located directly on a surface of* a gate dielectric, said Re-containing gate having an interface trapped charge density of about 3E 10 cm^{-2} eV^{-1} to about 4E 10 cm^{-2} eV^{-1} and a work function ranging from about 4.6 eV to about 5.0 eV, as recited in amended Claims 1, 10 and 17. Specifically, Talwar et al. does not disclose selecting the material of the gate conductor to tailor the work function of the gate region. Finally, Talwar et al. does not teach or suggest a semiconductor structure including a gate stack of a Re-containing gate and a gate dielectric selected from the group consisting of HfO_2, ZrO_3, Y_2O_3, silicates or nitrogen additions of HfO_2, ZrO_3, or Y_2O_3, and mixtures thereof. In Talwar et al., gate dielectric 8 is composed of silicon oxide, silicon nitride, aluminum oxide, titanium oxide, barium strontium oxide and tantalum oxide.

Therefore, because Talwar et al. fails to teach or suggest at least three limitations of Applicants' claimed structure, as recited in amended Claims 1, 10 and 17, Talwar et al. does not render Applicants' invention unpatentable.

Additionally, Applicants submit that one of ordinary skill in the art would not combine the disclosure of Talwar et al. with Suguro in a manner that would provide a structure that would meet all the limitations of Applicants' claims, as recited in amended Claims 1, 10 and 17. Applicants submit that in the unlikely event that one of ordinary skill in the art was to combine the disclosure of Talwar et al. with Suguro, the resultant structure would include the metal nitride layer 61 positioned between the metal gate and the gate dielectric, since the only disclosure of

material selection to control work function of the gate structure in the applied prior art is found in Columns 11, 12, and Figure 7b of the Suguro reference. Therefore, since the combination of Talwar et al. and Suguro would require the metal nitride layer present between the gate conductor and the gate dielectric, the combination of the applied prior art fails to teach or suggest a structure including a Re-containing gate located directly on a surface of a gate dielectric which has a work function ranging from about 4.6 eV to about 5.0 eV, as required by amended Claims 1, 10 and 17. Further, because the combination of Suguro and Talwar et al. fails to teach or suggest that the Re metal gate is located directly on a surface of the gate dielectric, the applied prior art fails to teach or suggest a Re-containing gate having an interface trapped charge density of about 3E 10 cm^{-2} eV^{-1} to about 4E 10 cm^{-2} eV^{-1}, as recited in amended Claims 1, 10 and 17.

Huang et al. also fails to fulfill the deficiencies of Suguro and Talwar et al., since the applied prior art reference fails to teach or suggest each and every limitation of Applicants' claimed structure. Similar to Suguro and Talwar et al., Huang et al. fails to teach or suggest a structure that includes a Re-containing gate that is located directly on a surface of the gate dielectric, wherein the Re-containing gate has an interface trapped charge density of about 3E 10 cm^{-2} eV^{-1} to about 4E 10 cm^{-2} eV^{-1}, and a work function ranging from about 4.6 eV to about 5.0 eV, as recited in amended Claims 1, 10 and 16. Applicants note that Huang et al. is directed to a thermal annealing method and is far removed from Applicants' invention.

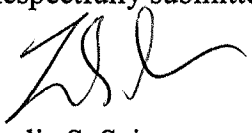
Referring to Page 3 of the present Office Action, it is the Examiner's position that the hydrogen annealing temperature and pressure taught by the Huang et al. reference when applied to the structures disclosed in Suguro and Talwar et al. would passivate the surface of the structures and result in Applicants' claimed interface trapped charge density. Applicants respectfully disagree, because none of the applied prior art references meet the limitation of a

Re-containing gate that is located directly on a surface of the gate dielectric and has a work function ranging from about 4.6 eV to about 5.0 eV, as recited in amended Claims 1, 10, and 13.

The rejections under 35 U.S.C. § 103 have been obviated; therefore reconsideration and withdrawal thereof are respectfully requested.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,



Leslie S. Szivos
Registration No. 39,394

Scully, Scott, Murphy & Presser, PC
400 Garden City Plaza, Suite 300
Garden City, New York 11530
(516) 742-4343

LSS:HAH:reg